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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/536,904	11/18/2005	Harumichi Mori	046124-5386	6567
23973 7590 03/29/2007 DRINKER BIDDLE & REATH ATTN: INTELLECTUAL PROPERTY GROUP ONE LOGAN SQUARE 18TH AND CHERRY STREETS PHILADELPHIA, PA 19103-6996			EXAMINER BAKER, DAVID S	
			ART UNIT 2884	PAPER NUMBER
SHORTENED STATUTORY PERIOD OF RESPONSE		MAIL DATE	DELIVERY MODE	
3 MONTHS		03/29/2007	PAPER	

**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

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<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/536,904	MORI ET AL.	
	<b>Examiner</b>	<b>Art Unit</b>	
	David S. Baker	2884	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 27 May 2005.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-11 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-11 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 27 May 2005 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date: _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)  | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date <u>11/18/05</u> | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).
3. Claims 1-3 and 9-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka (JP 62-086756 A) in view of Pan (US 6,351,002 B1).

Regarding claim 1, Tanaka discloses a solid state imaging apparatus comprising: an array of pn junction photodiodes (F:1a, abstract, C:1 L:1 thru C:8 L:8); and an electroconductive member covering the array of pn junction photodiodes (F:1a, abstract, C:1 L:1 thru C:8 L:8). Tanaka does not disclose expressly that the electroconductive member is grounded or held at a fixed potential. Pan discloses an array of pn junction photodiodes with an electroconductive member disposed on the photodiodes that is grounded (F:2, C:3 L:50 thru C:4 L:67). At the time the invention was made, it would

have been obvious to use the teaching of the grounded electroconductive protection of Pan in order to ground the electroconductive member of Tanaka. The motivation for doing so would have been that by grounding the electroconductive member, a decrease in excess charge buildup as well as a decrease in leakage current could be achieved; this reasoning is taught by Pan (C:3 L:50 thru C:4 L:67).

Regarding claim 2, Tanaka discloses that the electroconductive member is of a grid shape when viewed from a direction of incident light to the photosensitive section (F:1a-3b, abstract, C:1 L:1 thru C:8 L:8), and is provided so as to cover the pn junction portions exposed on the one side of the semiconductor substrate and portions between the second conductivity type semiconductor regions adjacent to each other (F:1a-3b, abstract, C:1 L:1 thru C:8 L:8).

Regarding claim 3, Pan discloses an array of pn junction photodiodes wherein an isolated region is formed between the second conductivity type semiconductor regions adjacent to each other (F:2, C:3 L:50 thru C:4 L:67), wherein an electroconductive member is electrically connected to the isolation region (F:2, C:3 L:50 thru C:4 L:67).

Regarding claim 9, Tanaka discloses a solid state imaging apparatus comprising: an array of pn junction photodiodes (F:1a, abstract, C:1 L:1 thru C:8 L:8); and an electroconductive member covering the array of pn junction photodiodes (F:1a, abstract, C:1 L:1 thru C:8 L:8). Tanaka does not disclose expressly that the electroconductive member for discharging a charge generated in a region except for the photodiodes to the outside. Pan discloses an array of pn junction photodiodes with an electroconductive member disposed on the photodiodes as well as in between the photodiodes that is

grounded (F:2, C:3 L:50 thru C:4 L:67) for discharging a charge to the outside. At the time the invention was made, it would have been obvious to use the teaching of the grounded electroconductive protection of Pan in order to ground the electroconductive member of Tanaka. The motivation for doing so would have been that by grounding the electroconductive member, a decrease in excess charge buildup as well as a decrease in leakage current could be achieved; this is taught by Pan (C:3 L:50 thru C:4 L:67).

Regarding claim 10, Pan discloses that an electroconductive member disposed on the photodiodes is grounded (F:2, C:3 L:50 thru C:4 L:67).

4. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka (JP 62-086756 A), Pan (US 6,351,002 B1), and further in view of Mizuno (US 6,384,396 B1).

Regarding claim 4, Tanaka and Pan disclose all the claimed limitations but do not disclose expressly signal lines for readout outputs, a switch group, or wires connected to control terminals of the respective switches. Mizuno discloses a solid state imaging device that comprises: a two dimensional array of photodiodes (F:1-4, C:3 L:20 thru C:8 L:9); signal lines for readout of the outputs from the photodiodes (F:1-4, C:3 L:20 thru C:8 L:9); a switch group consisting of a plurality of switches for controlling electrical connection and disconnection between each photodiode and the signal line in each column of the photodiodes (F:1-4, C:3 L:20 thru C:8 L:9); and wires connected to control terminals of the respective switches forming the switch group (F:1-4, C:3 L:20 thru C:8 L:9), and arranged to supply a scan signal to turn each switch off or on in each row of the photodiodes to the control terminals (F:1-4, C:3 L:20 thru C:8 L:9). Mizuno does not disclose expressly wherein the wires are located above the electroconductive member. At

the time the invention was made, it would have been obvious to a person of ordinary skill in the art to combine the two-dimensional array of photodiodes of Tanaka and Pan with the readout circuitry of Mizuno. The motivation for doing so would have been that by using the readout circuitry of Mizuno, the photodiode array of Tanaka and Pan could benefit from decreased dead zones and have an increased detection area. Additionally, at the time the invention was made, it would have been obvious to a person of ordinary skill in the art to locate the wires above the electroconductive member. The motivation for doing so would have been to provide for improved access to the circuit elements should any become damaged and need repaired.

5. Claims 5-8 rejected under 35 U.S.C. 103(a) as being unpatentable over Mizuno (US 6,384,396 B1) in view of Tanaka (JP 62-086756 A) and further in view of Pan (US 6,351,002 B1).

Regarding claim 5, Mizuno discloses a solid-state imaging apparatus comprising: a photosensitive section comprising a semiconductor substrate of a first conductivity type (F:1-4, C:3 L:20 thru C:8 L:9), and a plurality of second conductivity type semiconductor regions arrayed in a matrix of M rows and N columns on one side of the semiconductor substrate (F:1-4, C:3 L:20 thru C:8 L:9), wherein the semiconductor substrate and each second conductivity type semiconductor region constitute a pn junction to function as a photodiode (F:1-4, C:3 L:20 thru C:8 L:9); first wires provided in the respective columns (F:1-4, C:3 L:20 thru C:8 L:9); a first switch group consisting of a plurality of switches for connection between each photodiode and the first wire in each column (F:1-4, C:3 L:20 thru C:8 L:9); a vertical shift register for outputting a vertical scan signal to open

and close each switch forming the first switch group, in each row (F:1-4, C:3 L:20 thru C:8 L:9); second wires for connecting control terminals of the respective switches forming the first switch group, to the vertical shift register in each row (F:1-4, C:3 L:20 thru C:8 L:9); a second switch group consisting of a plurality of switches for connection between each first wire and a signal output line (F:1-4, C:3 L:20 thru C:8 L:9); a horizontal shift register for outputting a horizontal scan signal to open and close each switch forming the second switch group, in each column (F:1-4, C:3 L:20 thru C:8 L:9). Mizuno does not disclose expressly an electroconductive member provided so as to cover at least the pn junction portions exposed on the one side of the semiconductor substrate, or wherein the electroconductive member is connected to a fixed potential, or is grounded. Tanaka discloses an electroconductive member covering an array of pn junction photodiodes (F:1a, abstract, C:1 L:1 thru C:8 L:8). Pan discloses an array of pn junction photodiodes with an electroconductive member disposed on the photodiodes that is grounded (F:2, C:3 L:50 thru C:4 L:67). At the time the invention was made, it would have been obvious to use the electroconductive member of Tanaka to cover over the pn junction photodiode array of Mizuno. The motivation for doing so would have been to provide a protective layer over the pn junction photodiode array as well as a way to reduce leakage current. Additionally, at the time the invention was made, it would have been obvious to a person of ordinary skill in the art to use the teaching of the grounded electroconductive protection of Pan in order to ground the electroconductive member of Tanaka on the photodiode array of Mizuno. The motivation for doing so would have been that by grounding the electroconductive member, a decrease in excess charge

buildup as well as a further decrease in leakage current could be achieved; this reasoning is taught by Pan (C:3 L:50 thru C:4 L:67).

Regarding claim 6, Tanaka discloses that the electroconductive member is of a grid shape when viewed from a direction of incident light to the photosensitive section (F:1a-3b, abstract, C:1 L:1 thru C:8 L:8), and is provided so as to cover the pn junction portions exposed on the one side of the semiconductor substrate and portions between the second conductivity type semiconductor regions adjacent to each other (F:1a-3b, abstract, C:1 L:1 thru C:8 L:8).

Regarding claim 7, Pan discloses an array of pn junction photodiodes wherein an isolated region is formed between the second conductivity type semiconductor regions adjacent to each other (F:2, C:3 L:50 thru C:4 L:67), wherein an electroconductive member is electrically connected to the isolation region (F:2, C:3 L:50 thru C:4 L:67).

Regarding claim 8, Mizuno does not disclose expressly that the wires are located above the electroconductive member. At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to locate the wires above the electroconductive member. The motivation for doing so would have been to provide for improved access to the circuit elements should any become damaged and need repaired.

6. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka (JP 62-086756 A), Pan (US 6,351,002 B1), and further in view of Tashiro (US 2002/0017611 A1).

Regarding claim 11, Tanaka and Pan disclose all the claimed limitations but do not disclose expressly a scintillator for converting radiation to visible light which is provides so as to cover the plurality of photodiodes. Tashiro discloses a scintillator for



converting radiation to visible light which is provides so as to cover a two dimensional array of photodiodes (F:4, P:0055-0056). At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to provide the scintillator of Tashiro to convert radiation to visible light for detection by the photodiode array of Tanaka and Pan. The motivation for doing so would have been to improve the wavelength range over which the detection of radiation could be achieved.

### *Conclusion*

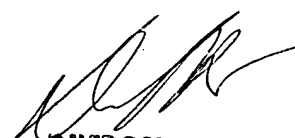
Any inquiry concerning this communication or earlier communications from the examiner should be directed to David S. Baker whose telephone number is (571) 272-6003. The examiner can normally be reached on MTWRF 9:30am-6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David P. Porta can be reached on (571) 272-2444. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Art Unit: 2884

DSB



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